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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/523,031	02/02/2005	Daniel Shane O'Sullivan	4403-40000US6	8713

27123 7590 04/04/2007

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EXAMINER	
FAHERTY, COREY S	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/523,031	O'SULLIVAN, DANIEL SHANE	
	Examiner	Art Unit	
	Corey S. Faherty	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *144,145,155-158,160,164,165 and 167-172* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *144,145,155-158,160,164,165 and 167-172* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02/02/2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 144-145, 155-158, 160, 164-165 and 167-172 have been examined.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

2. The drawings are objected to because the text on them is illegible. For instance, the text on Figures 1A, 1B, 3, 4 and others is not clear enough to be read easily. Applicant is required to submit new drawings such that all text is clear enough to be read easily. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR

1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 156 and 168-170 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 156 recites the limitation "the originating processing resource" in line 2. There insufficient antecedent basis for this limitation in the claim.

6. Claims 168-170 recite the limitation "the execution-instruction signal" in line 1. There is insufficient antecedent basis for this limitation in the claims.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 144, 155-156, 164-165 and 167-170 are rejected under 35 U.S.C. 102(b) as being anticipated by Bonola (U.S. Patent 5,706,514).

9. Regarding claim 144, Bonola discloses a method of execution-instruction delegation between processing resources [abstract], comprising: obtaining an execution instruction, wherein the execution instruction is obtained at a processing resource [col. 3, line 26; a command is encountered]; determining whether an operation-code within the execution instruction should be delegated to an other processing resource [col. 3, lines 25-29; it is determined if the instruction is a type that cannot currently be executed by the host processor]; executing the execution instruction, if the operation-code within the execution instruction should not be delegated to an other processing resource [col. 3, lines 23-44; if the encountered instruction is not of a type that cannot currently be executed by the host processor, the host processor continues executing it normally]; routing the execution instruction to an other processing resource, if the operation-code within the execution instruction is for an other processing resource [col. 3, lines 36-51; when an encountered instruction is of a type that cannot currently be executed by the host processor, the host processor transfers data to a slave processor's registers so that the slave processor may execute the instruction].

10. Regarding claim 155, Bonola discloses the method of claim 144, wherein the operation-code indicates a type of resource on which to execute [col. 3, lines 25-30; an instruction specifies a certain mode of processor on which it can executed].

11. Regarding claim 156, Bonola discloses the method of claim 144, wherein the other processing resource may be the originating processing resource [col. 3, lines 23-44; if the

encountered instruction is not of a type that cannot currently be executed by the host processor, the host processor continues executing it normally].

12. Regarding claim 164, Bonola discloses the method of claim 144, wherein a processing resource is an execution-instruction processing cache [col. 3, lines 37-42; the slave processor's registers are used to temporarily hold all data that is necessary for the slave processor to perform the execution provided to it by the host processor].

13. Regarding claim 165, Bonola discloses the method of claim 144, wherein routing occurs through an execution-instruction signal router [col. 3, lines 37-42; the slave processor's registers are used to temporarily hold all data that is necessary for the slave processor to perform the execution provided to it by the host processor; Fig. 1; col. 4, lines 43-45; a host bus is also provided to allow the host processor to communicate with the slave processors].

14. Regarding claim 167, Bonola discloses the method of claim 144, wherein a processing resource may sleep while an other processing resource executes delegated execution-instructions [col. 8, lines 55-61; col. 9, lines 64-66; a slave processor may enter a sleep mode while the host processor or other slave processors execute instructions].

15. Regarding claim 168, Bonola discloses the method of claim 144, wherein the execution-instruction signal causes various processing resources dynamically to turn on and off [col. 8, lines 55-61; col. 9, lines 64-66; slave processors may enter a sleep mode in which they do not execute instructions].

16. Regarding claim 169, Bonola discloses the method of claim 144, wherein the execution-instruction signal from processing resources themselves shuts off processing resources while

idling [col. 8, lines 55-61; col. 9, lines 64-66; slave processors may enter a sleep mode in which they do not execute instructions].

17. Regarding claim 170, Bonola discloses the method of claim 144, wherein the execution-instruction signal from processing resources themselves turn on processing resources when execution-instruction signal processing is required [col. 8, lines 55-61; col. 9, lines 64-66; a slave processor may be removed from sleep mode when it is necessary for executing instructions that the host processor is unable to execute].

18. Claims 144 and 171-172 are rejected under 35 U.S.C. 102(e) as being anticipated by Butterworth et al. (U.S. Patent 6,907,454), referenced from here forward as Butterworth.

19. Regarding claim 144, Butterworth discloses a method of execution-instruction delegation between processing resources [abstract], comprising: obtaining an execution instruction, wherein the execution instruction is obtained at a processing resource [col. 2, lines 48-50; a master processor receives a memory access instruction]; determining whether an operation-code within the execution instruction should be delegated to an other processing resource [col. 2, lines 48-54; the master processor determines that an instruction is of a memory access type and, if it is, determines that it should be sent to a slave processor]; executing the execution instruction, if the operation-code within the execution instruction should not be delegated to an other processing resource [col. 2, lines 44-58; the master processor executes non-memory access instructions normally]; routing the execution instruction to an other processing resource, if the operation-code within the execution instruction is for an other processing resource [col. 2, lines 53-54; for memory access instructions, the master processor writes a request to the slave processor to carry out the instruction].

20. Regarding claim 171, Butterworth discloses the method of claim 144, wherein processing resources are communicatively disposed on a same die [col. 4, lines 36-40; a bridge device for communication between the memory and the slave processor may be integrated into a single chip package with the slave processor].

21. Regarding claim 172, Butterworth discloses the method of claim 171, wherein an execution-instruction signal router is on the same die with processing resources [col. 4, lines 36-40; a bridge device for communication between the memory and the slave processor may be integrated into a single chip package with the slave processor].

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

24. Claim 145 is rejected under 35 U.S.C. 103(a) as being unpatentable over Butterworth.

25. Regarding claim 145, Butterworth discloses the method of claim 145, but does not explicitly disclose that the method is completed within a single processing cycle.

The purpose of the Butterworth design is to reduce the processing delay of a memory operation [col. 1, lines 59-65]. Instead of forcing a processor to incur all of the delay necessary for executing a memory operation, the processor instead delegates the operation to a second processor [col. 2, lines 44-58]. If the first processor is able to perform this delegation quickly, it can continue executing other instructions [col. 5, lines 50-51] while the second processor performs the memory operation. The fewer clock cycles it takes for the first processor to perform the delegation, the more time the first processor will have to execute other instructions while the second processor is performing the memory operation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to complete the instruction-delegation method disclosed in Butterworth in a single processing cycle because doing so would allow the master processor to begin executing other instructions more quickly and thus execute more code overall while the slave processor is performing a memory operation.

26. Claims 157-158 and 160 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bonola as applied to claim 144 above, and further in view of Mohamed et al. (U.S. Patent 5,978,838), referenced from here forward as Mohamed.

27. Regarding claim 157, Bonola does not explicitly disclose that a processing resource is an integer-processing unit.

Mohamed discloses a system similar to that of Bonola in which two processors interact to efficiently process instructions [col. 1, lines 61-67]. The system includes integer-processing units for executing integer instructions [col. 5, lines 8-15].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an integer-processing unit as a processing resource in the system of Bonola because Mohamed discloses doing including an integer-processing unit in a multi-processor system [col. 5, lines 8-15] and doing so allows the system to execute integer instructions. Furthermore, without an integer-processing unit, the system of Bonola would be unable to execute integer instructions, greatly limiting the amount of software that it could run.

28. Regarding claim 158, Bonola does not explicitly disclose that a processing resource is a mathematical processing unit.

Mohamed discloses a system similar to that of Bonola in which two processors interact to efficiently process instructions [col. 1, lines 19-26]. The system includes a math co-processor [col. 1, line 24].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a mathematical processing unit as a processing resource in the system of Bonola because Mohamed discloses including a math processor in a multi-processor system [col. 1, lines 19-26] and doing so allows the system to more efficiently execute mathematical operations. The use of a mathematical processor as a slave processor in the system of Bonola allows the host processor to be designed for better execution of other types of instructions, allowing for greater overall processing efficiency. Furthermore, the addition of a mode in which

a slave processor behaves a mathematical processor allows the system of Bonola to execute mathematical operations, also potentially increasing overall processing efficiency.

29. Regarding claim 160, Bonola does not explicitly disclose that a processing resource is a vector-processing unit.

Mohamed discloses a system similar to that of Bonola in which two processors interact to efficiently process instructions [col. 1, lines 61-67]. The system includes a vector processor [abstract].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a vector-processing unit as a processing resource in the system of Bonola because Mohamed discloses including a vector processor in a multi-processor system [abstract] and doing so allows a system to more efficiently execute vector instructions without impacting the execution efficiency of a main processor. The addition of a vector processing mode to a slave processor in the system of Bonola would allow the host processor to delegate vector operations to slave processors while continuing to execute other instructions, resulting in greater processing efficiency.

Conclusion

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references are closely related to the subject matter of the instant application and should be fully considered in any reply to this Office Action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey S. Faherty whose telephone number is (571) 270-1319. The examiner can normally be reached on Monday-Thursday and every other Friday, 7:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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